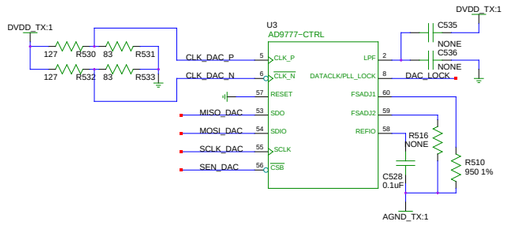
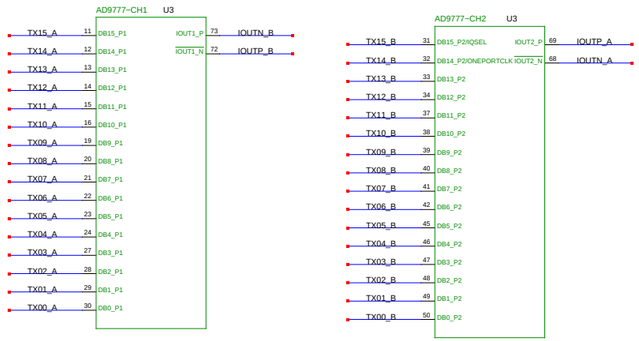
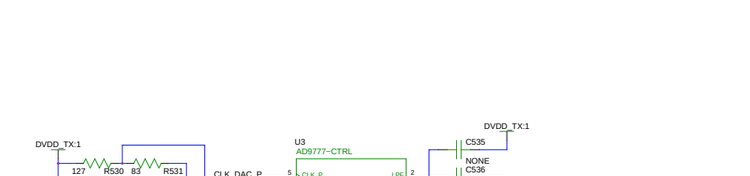
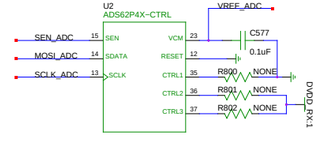
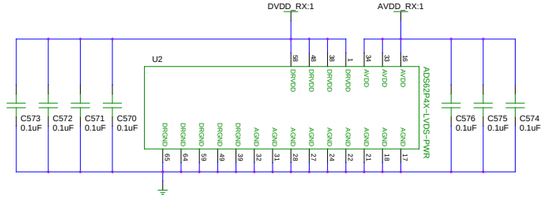






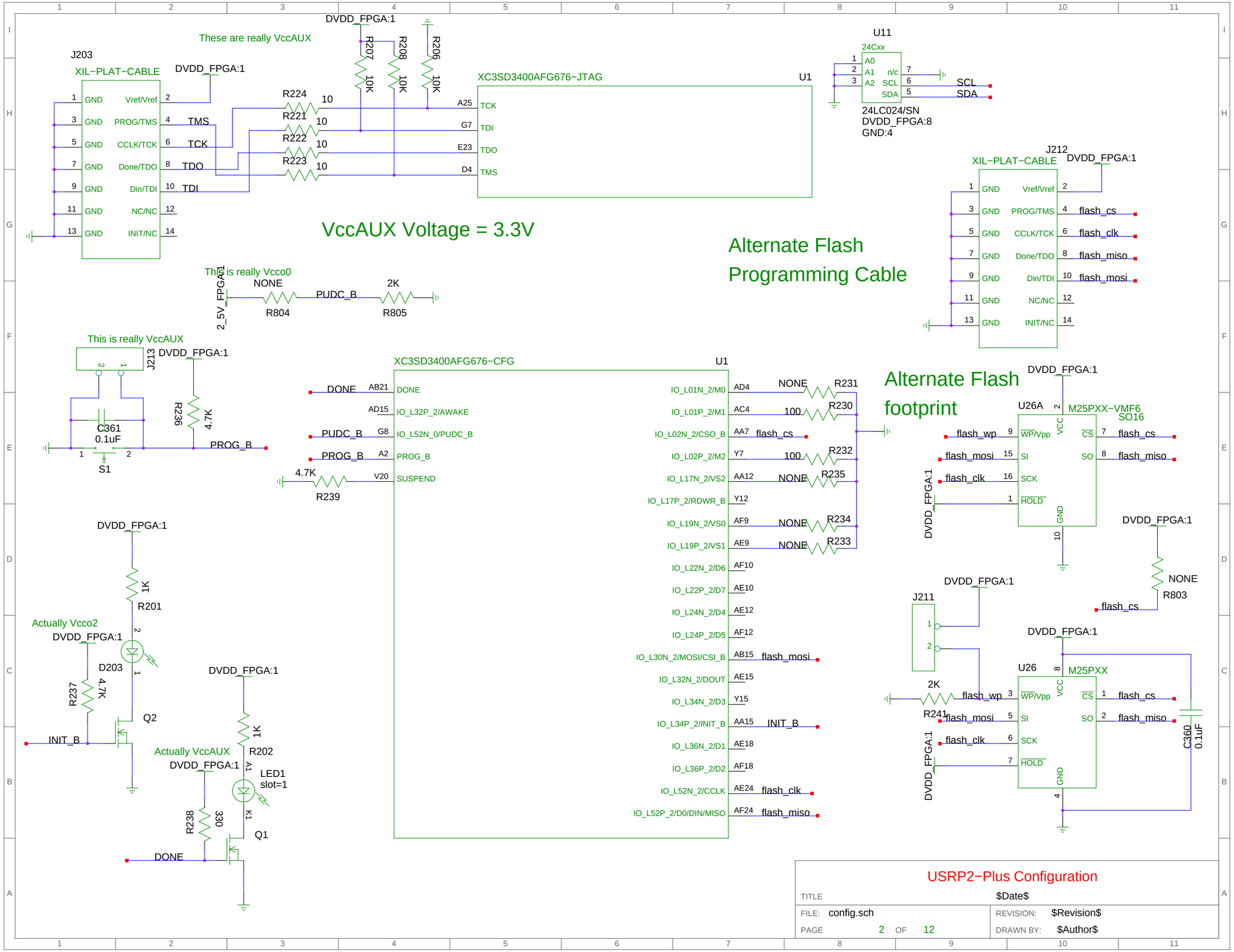
Inverted Input A to make routing easier
fix in FPGA

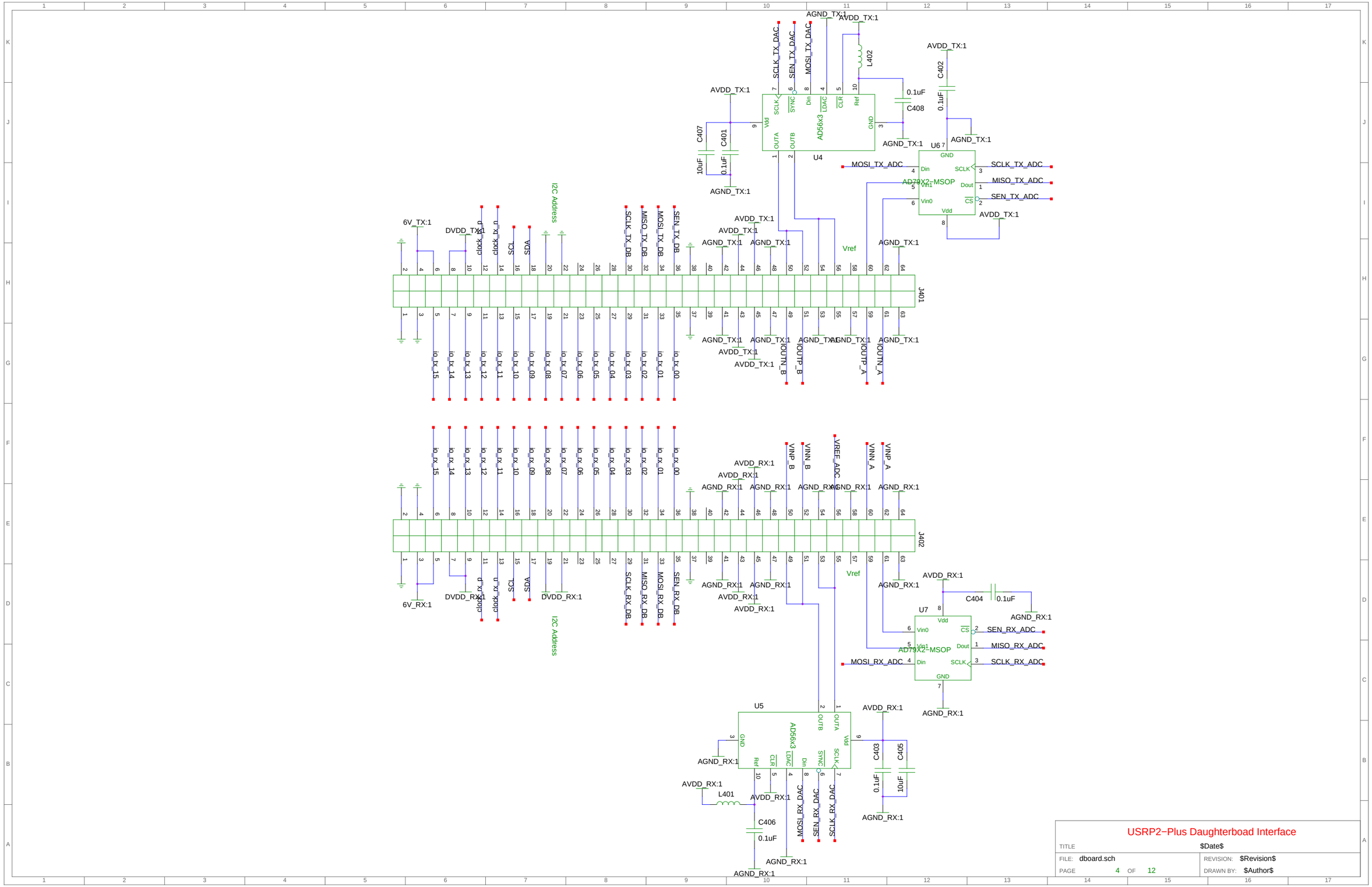




USRP2-Plus CODECs

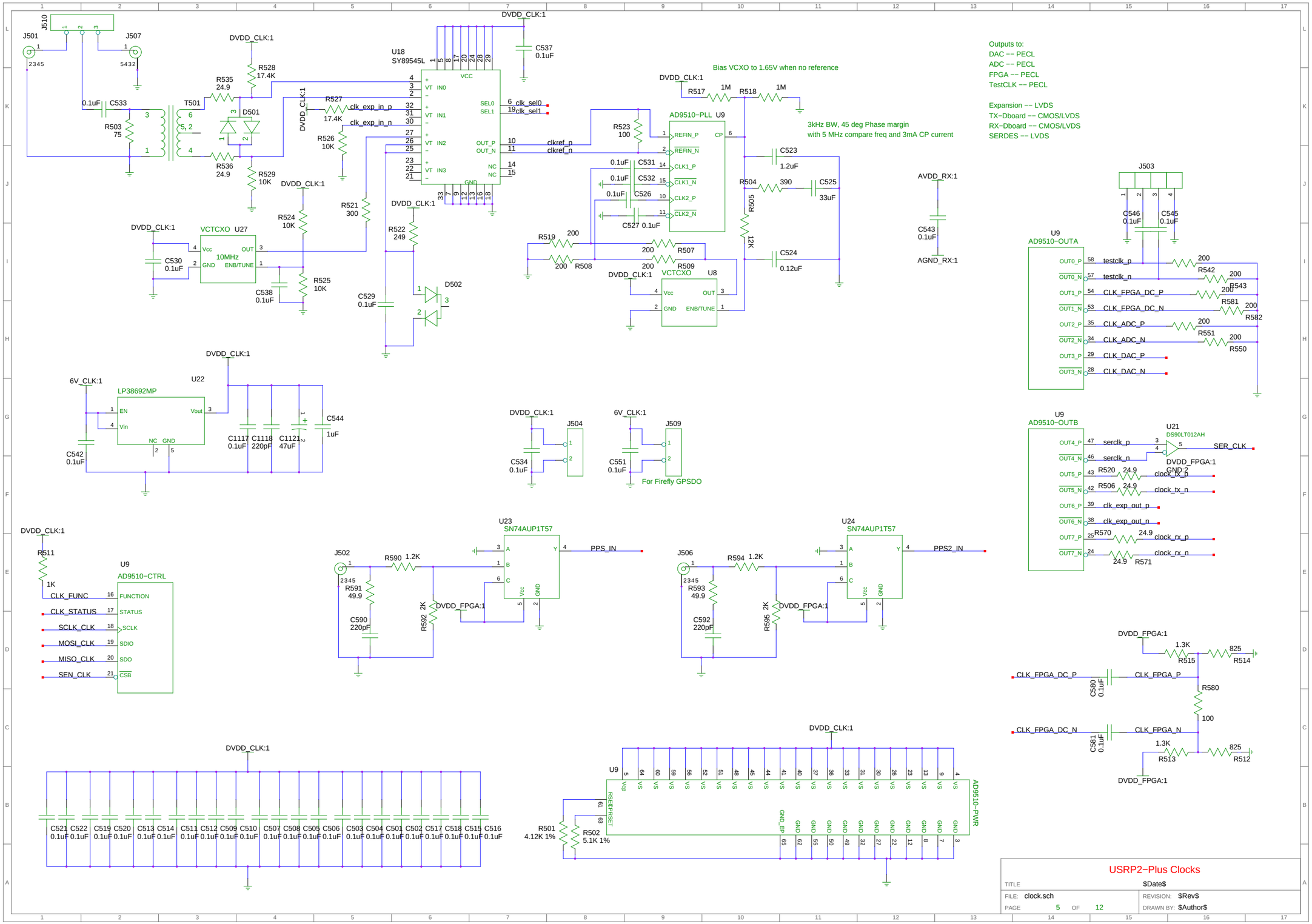
TITLE	$Date$
FILE: codecs.sch	REVISION: Rev
PAGE 3 OF 12	DRAWN BY: $Author$

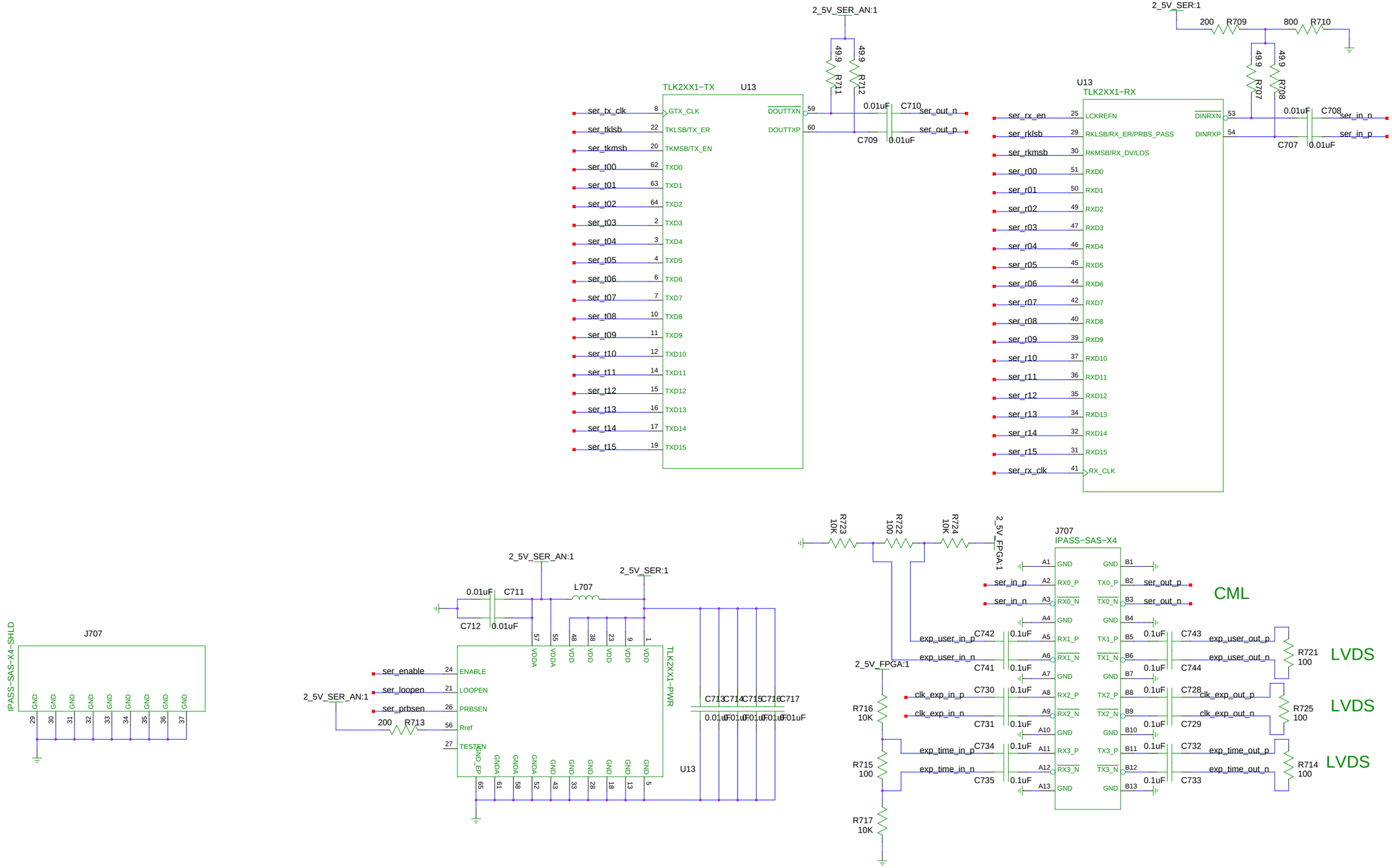

These are really VccAUX
DVDD_FPGA:1
R207 10K
R208 10K
R206 10K
J203
XIL−PLAT−CABLE
DVDD_FPGA:1
R224 10
R221 10
R222 10
R223 10
XC3SD3400AFG676−JTAG
U1
A25 TCK
G7 TDI
E23 TDO
D4 TMS
TMS
TCK
TDO
TDI
U11
24Cxx
A0
A1
A2
n/c
SCL
SDA
SCL
SDA
24LC024/SN
DVDD_FPGA:8
GND:4
VccAUX Voltage = 3.3V
Alternate Flash
Programming Cable
J212
XIL−PLAT−CABLE
DVDD_FPGA:1
flash_cs
flash_clk
flash_miso
flash_mosi
This is really Vcco0
2_5V_FPGA:1
NONE
R804
PUDC_B
2K
R805
This is really VccAUX
J213
DVDD_FPGA:1
C361
0.1uF
R236
4.7K
PROG_B
S1
XC3SD3400AFG676−CFG
U1
DONE AB21 DONE
AD15 IO_L32P_2/AWAKE
PUDC_B G8 IO_L52N_0/PUDC_B
PROG_B A2 PROG_B
4.7K V20 SUSPEND
R239
IO_L01N_2/M0 AD4
IO_L01P_2/M1 AC4
IO_L02N_2/CSO_B AA7 flash_cs
IO_L02P_2/M2 Y7
IO_L17N_2/VS2 AA12
IO_L17P_2/RDWR_B Y12
IO_L19N_2/VS0 AF9
IO_L19P_2/VS1 AE9
IO_L22N_2/D6 AF10
IO_L22P_2/D7 AE10
IO_L24N_2/D4 AE12
IO_L24P_2/D5 AF12
IO_L30N_2/MOSI/CSI_B AB15 flash_mosi
IO_L32N_2/DOUT AE15
IO_L34N_2/D3 Y15
IO_L34P_2/INIT_B AA15 INIT_B
IO_L36N_2/D1 AE18
IO_L36P_2/D2 AF18
IO_L52N_2/CCLK AE24 flash_clk
IO_L52P_2/D0/DIN/MISO AF24 flash_miso
NONE R231
100 R230
flash_cs
100 R232
NONE R235
NONE R234
NONE R233
Alternate Flash
footprint
DVDD_FPGA:1
U26A
M25PXX−VMF6
SO16
flash_wp
flash_mosi
flash_clk
flash_cs
flash_miso
WP/Vpp
SI
SCK
HOLD
CS
SO
VCC
GND
DVDD_FPGA:1
DVDD_FPGA:1
NONE
R803
flash_cs
DVDD_FPGA:1
J211
DVDD_FPGA:1
U26
M25PXX
2K
R241
flash_wp
flash_mosi
flash_clk
WP/Vpp
SI
SCK
HOLD
CS
SO
VCC
GND
flash_cs
flash_miso
C360
0.1uF
DVDD_FPGA:1
Actually Vcco2
DVDD_FPGA:1
1K
R201
D203
R237
4.7K
Q2
INIT_B
DVDD_FPGA:1
Actually VccAUX
DVDD_FPGA:1
1K
R202
LED1
slot=1
R238
330
Q1
DONE
USRP2−Plus Configuration
TITLE
$Date$
FILE: config.sch
REVISION: $Revision$
PAGE 2 OF 12
DRAWN BY: $Author$



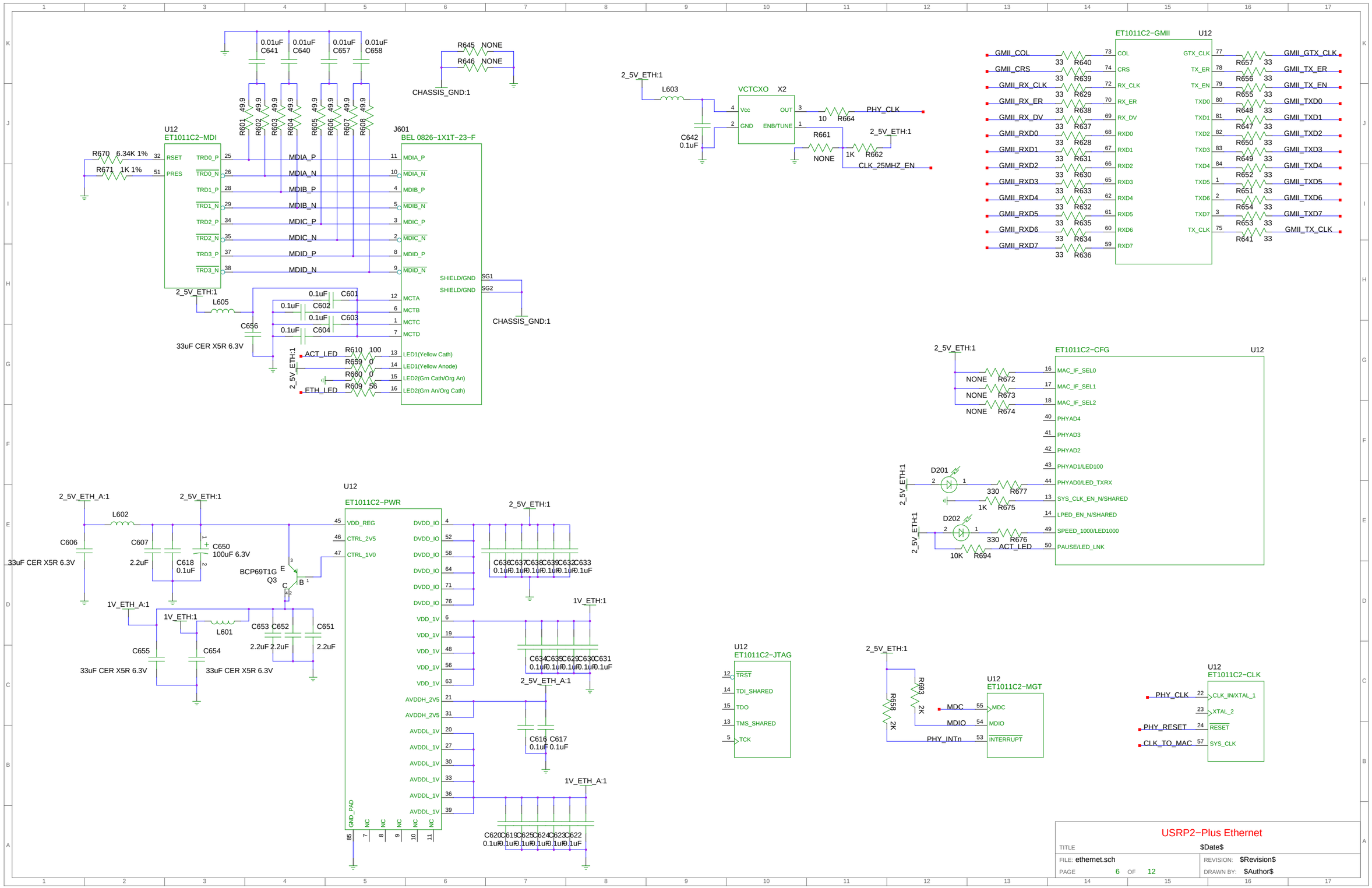
USRP2−Plus Daughterboad Interface

TITLE	$Date$
FILE: dboard.sch	REVISION: $Revision$
PAGE 4 OF 12	DRAWN BY: $Author$

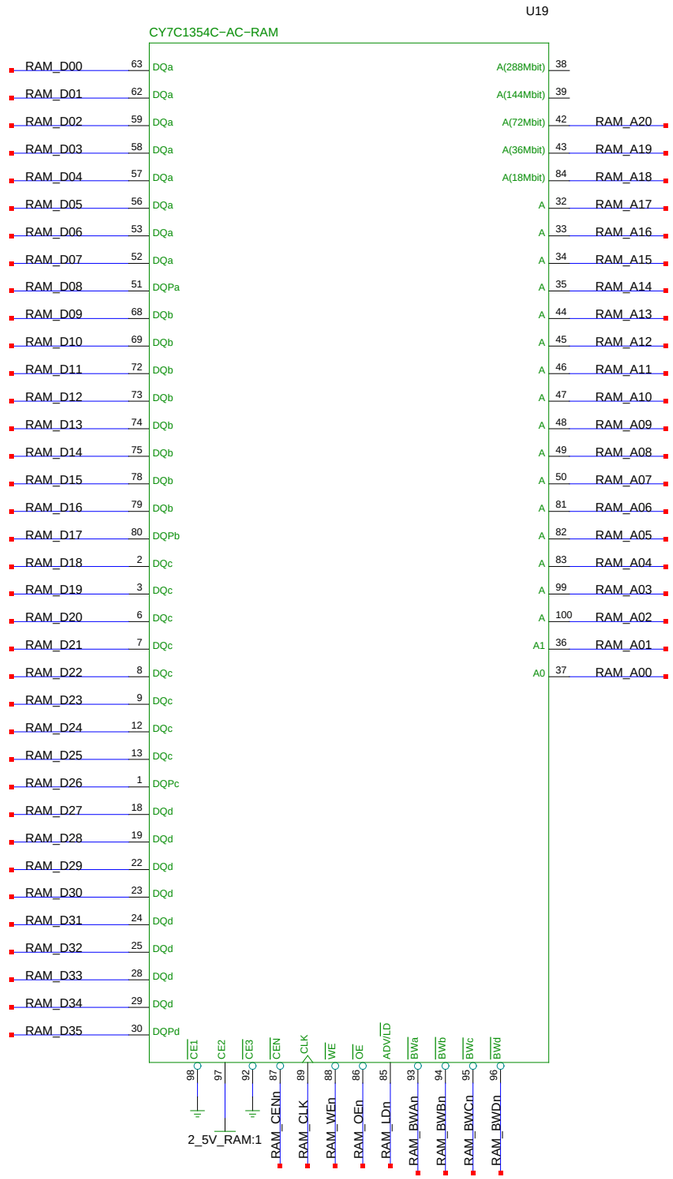

J510
J501
J507
2345
5432
0.1uF C533
R503 75
T501
R528 17.4K
R535 24.9
R536 24.9
D501
R529 10K
DVDD_CLK:1
R527 17.4K
R526 10K
clk_exp_in_p
clk_exp_in_n
U18
SY89545L
VCC
VT IN0
VT IN1
VT IN2
VT IN3
SEL0
SEL1
OUT_P
OUT_N
NC
GND
C537 0.1uF
clk_sel0
clk_sel1
clkref_p
clkref_n
R521 300
R524 10K
R522 249
C529 0.1uF
D502
VCTCXO U27
10MHz
Vcc
GND
OUT
ENB/TUNE
C530 0.1uF
C538 0.1uF
R525 10K
Bias VCXO to 1.65V when no reference
R517 1M
R518 1M
AD9510-PLL U9
REFIN_P
REFIN_N
CLK1_P
CLK1_N
CLK2_P
CLK2_N
CP
R523 100
C531 0.1uF
C532 0.1uF
C526 0.1uF
C527 0.1uF
R519 200
R508 200
R507 200
R509 200
VCTCXO U8
C523 1.2uF
R504 390
C525 33uF
R505 12K
C524 0.12uF
3kHz BW, 45 deg Phase margin
with 5 MHz compare freq and 3mA CP current
Outputs to:
DAC -- PECL
ADC -- PECL
FPGA -- PECL
TestCLK -- PECL
Expansion -- LVDS
TX-Dboard -- CMOS/LVDS
RX-Dboard -- CMOS/LVDS
SERDES -- LVDS
AVDD_RX:1
C543 0.1uF
AGND_RX:1
J503
C546 0.1uF
C545 0.1uF
U9
AD9510-OUTA
OUT0_P testclk_p
OUT0_N testclk_n
OUT1_P CLK_FPGA_DC_P
OUT1_N CLK_FPGA_DC_N
OUT2_P CLK_ADC_P
OUT2_N CLK_ADC_N
OUT3_P CLK_DAC_P
OUT3_N CLK_DAC_N
R542 200
R543 200
R581 200
R582 200
R551 200
R550 200
6V_CLK:1
U22
LP38692MP
EN
Vin
Vout
NC
GND
C542 0.1uF
C1117 0.1uF
C1118 220pF
C1121 47uF
C544 1uF
J504
C534 0.1uF
J509
C551 0.1uF
For Firefly GPSDO
U9
AD9510-OUTB
OUT4_P serclk_p
OUT4_N serclk_n
OUT5_P clock_tx_p
OUT5_N clock_tx_n
OUT6_P clk_exp_out_p
OUT6_N clk_exp_out_n
OUT7_P clock_rx_p
OUT7_N clock_rx_n
R520 24.9
R506 24.9
R570 24.9
R571 24.9
U21
DS90LT012AH
SER_CLK
DVDD_FPGA:1
GND:2
U9
AD9510-CTRL
CLK_FUNC FUNCTION
CLK_STATUS STATUS
SCLK_CLK SCLK
MOSI_CLK SDIO
MISO_CLK SDO
SEN_CLK CSB
R511 1K
J502
R590 1.2K
R591 49.9
C590 220pF
R592 2K
U23
SN74AUP1T57
PPS_IN
J506
R594 1.2K
R593 49.9
C592 220pF
R595 2K
U24
SN74AUP1T57
PPS2_IN
DVDD_FPGA:1
CLK_FPGA_DC_P
CLK_FPGA_N
C580 0.1uF
R580 100
CLK_FPGA_DC_N
C581 0.1uF
R515 1.3K
R514 825
R513 1.3K
R512 825
C521 0.1uF
C522 0.1uF
C519 0.1uF
C520 0.1uF
C513 0.1uF
C514 0.1uF
C511 0.1uF
C512 0.1uF
C509 0.1uF
C510 0.1uF
C507 0.1uF
C508 0.1uF
C505 0.1uF
C506 0.1uF
C503 0.1uF
C504 0.1uF
C501 0.1uF
C502 0.1uF
C517 0.1uF
C518 0.1uF
C515 0.1uF
C516 0.1uF
U9
AD9510-PWR
Vcp
VS
RSET
EPRSET
GND_EP
GND
R501 4.12K 1%
R502 5.1K 1%
USRP2-Plus Clocks
TITLE $Date$
FILE: clock.sch
REVISION: Rev
PAGE 5 OF 12
DRAWN BY: $Author$



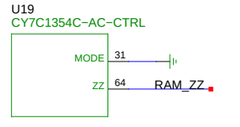
TITLE	USRP2−Plus Expansion
	$Date$
FILE: expansion.sch	REVISION: $Revision$
PAGE 7 OF 12	DRAWN BY: $Author$

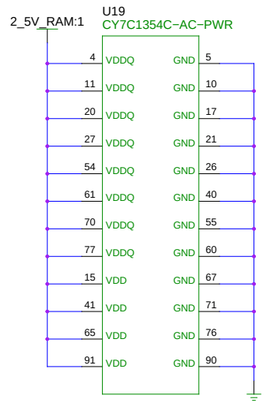


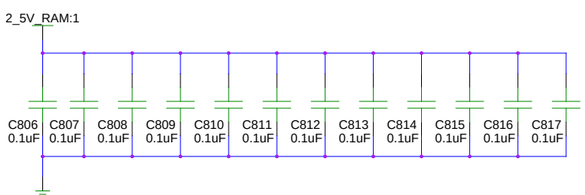
TITLE	USRP2−Plus Ethernet
	$Date$
FILE: ethernet.sch	REVISION: $Revision$
PAGE 6 OF 12	DRAWN BY: $Author$



FIXME −− Extra Power Supply Pins for IDT Version?







USRP2−Plus RAM

TITLE	$Date$
FILE: ram.sch	REVISION: Rev
PAGE 8 OF 12	DRAWN BY: $Author$

Bank 0, 2.5V
RAM

Removed Vcco0 due to bug in gnetlist

U1

XC3SD3400AFG676-I-IO3

2_5V_FPGA-1

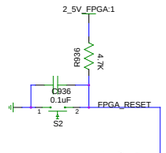
XC3SD3400AFG676-TOPCLK

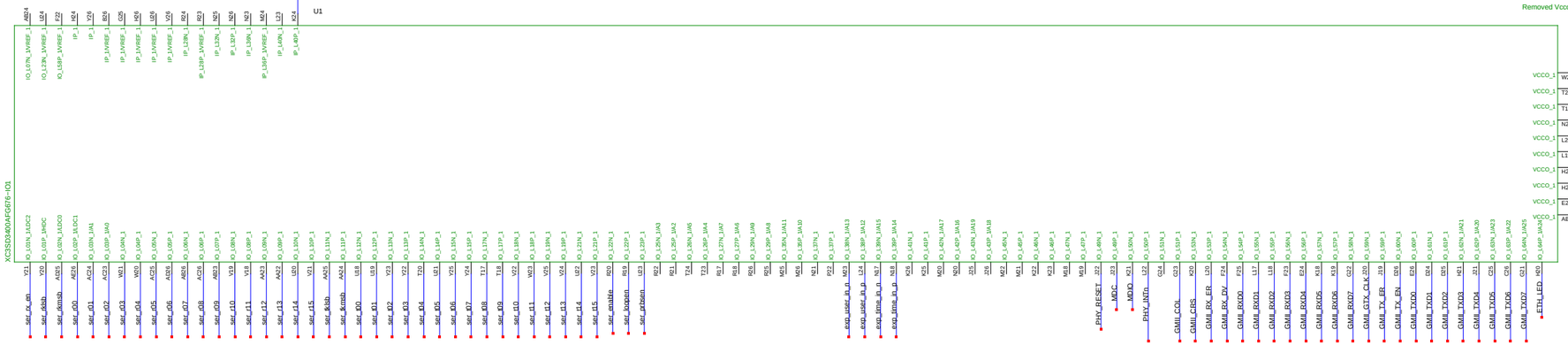
U1

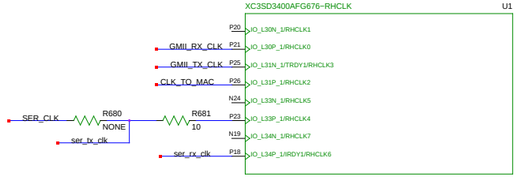
USRP2-Plus FPGA Bank 0

TITLE:	$Date$
FILE: fpga-bank0.sch	REVISION: Rev
PAGE: 9 OF 12	DRAWN BY: $Author$

Bank 1, 2.5V
No LVDS Out
Ethernet
SERDES
Expansion LVDS in

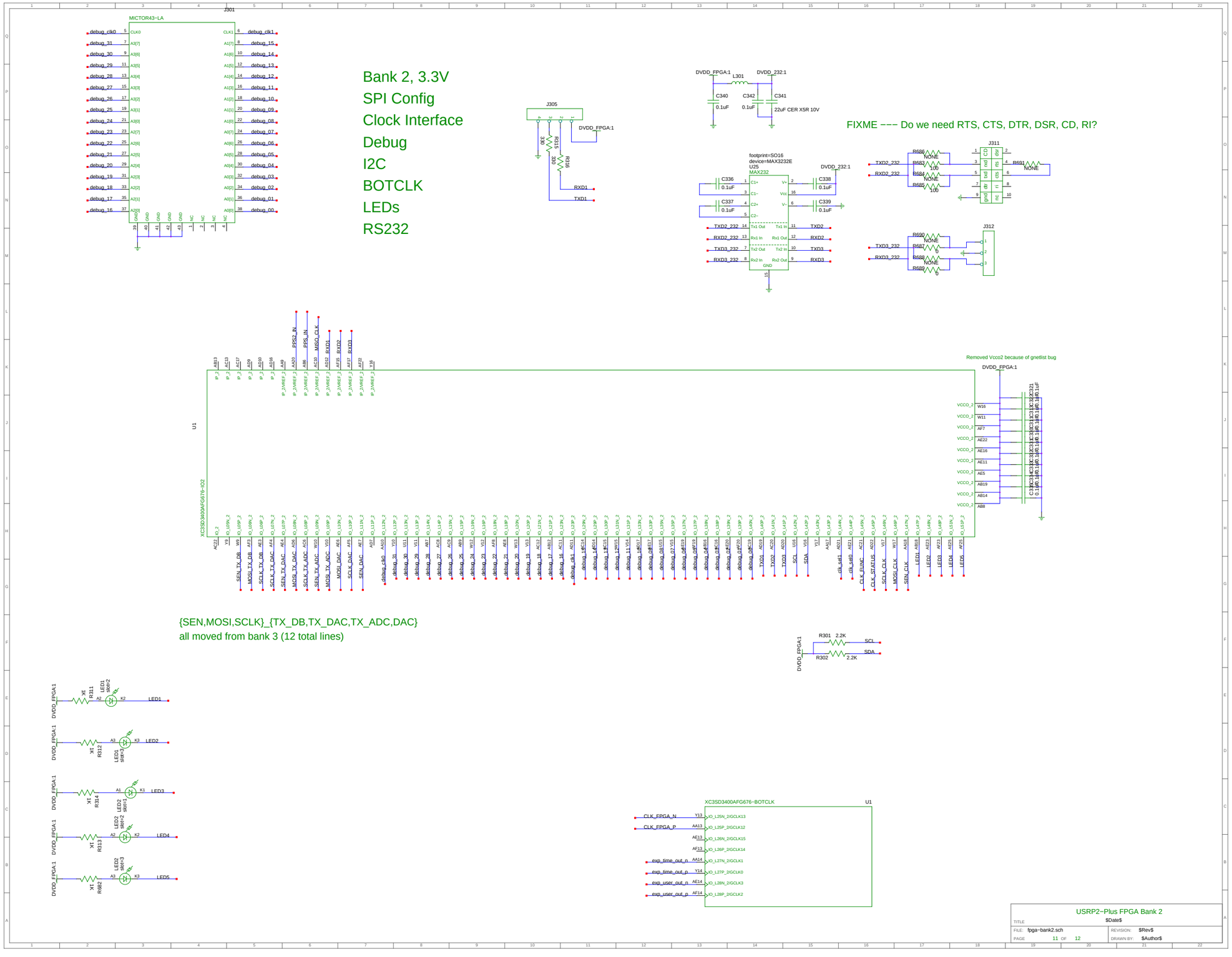






USRP2-Plus FPGA Bank 1

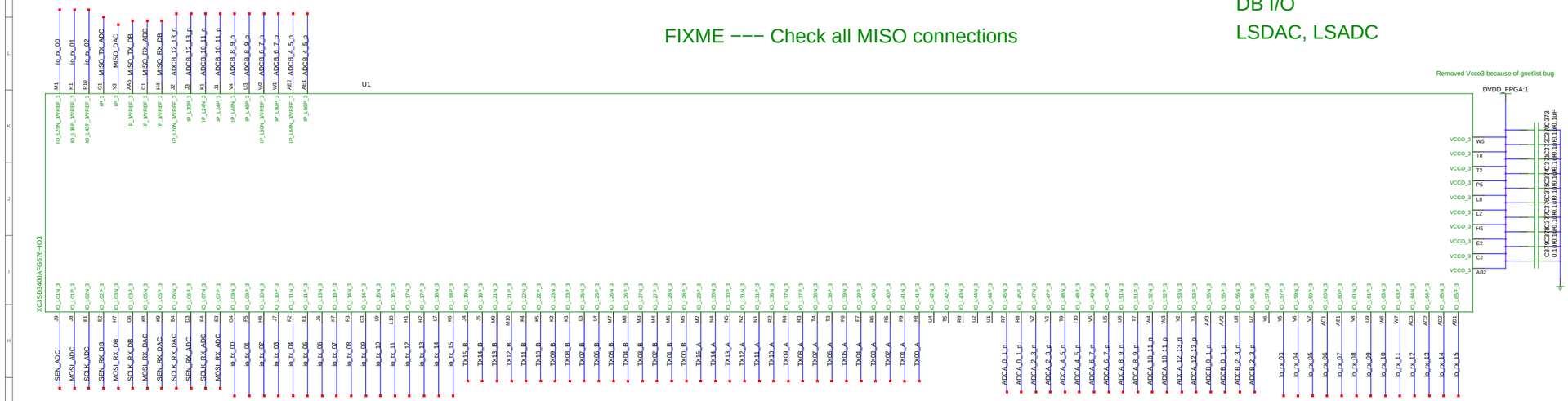
TITLE: $Date$	
FILE: fpga-bank1.sch	REVISION: Rev
PAGE 10 OF 12	DRAWN BY: $Author$

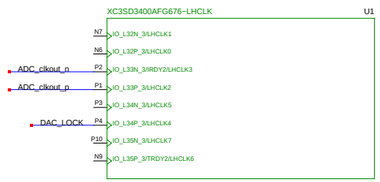

J301
MICTOR43-LA
debug_clk0
debug_31
debug_30
debug_29
debug_28
debug_27
debug_26
debug_25
debug_24
debug_23
debug_22
debug_21
debug_20
debug_19
debug_18
debug_17
debug_16
debug_clk1
debug_15
debug_14
debug_13
debug_12
debug_11
debug_10
debug_09
debug_08
debug_07
debug_06
debug_05
debug_04
debug_03
debug_02
debug_01
debug_00
Bank 2, 3.3V
SPI Config
Clock Interface
Debug
I2C
BOTCLK
LEDs
RS232
J305
DVDD_FPGA:1
R315
30
R316
30
RXD1
TXD1
DVDD_FPGA:1
L301
DVDD_232:1
C340
0.1uF
C342
0.1uF
C341
22uF CER X5R 10V
FIXME --- Do we need RTS, CTS, DTR, DSR, CD, RI?
footprint=SO16
device=MAX3232E
U25
MAX232
C336
0.1uF
C337
0.1uF
C338
0.1uF
C339
0.1uF
TXD2_232
RXD2_232
TXD3_232
RXD3_232
TXD2
RXD2
TXD3
RXD3
J311
R686
R683
R684
R685
R691
NONE
100
J312
R690
R687
R688
R689
0
U1
XC3SD3400AFG676-I02
PDS2_FI
PDS_IN
MSO_CLK
RXD1
RXD2
RXD3
Removed Vcco2 because of gnetlist bug
DVDD_FPGA:1
C321
0.1uF
SEN_TX_DB
MOSI_TX_DB
SCLK_TX_DB
SEN_TX_DAC
MOSI_TX_DAC
SCLK_TX_DAC
SEN_TX_ADC
MOSI_TX_ADC
SCLK_TX_ADC
SEN_DAC
MOSI_DAC
SCLK_DAC
SEN_DAC
debug_clk0
debug_clk1
debug_31
debug_30
debug_29
debug_28
debug_27
debug_26
debug_25
debug_24
debug_23
debug_22
debug_21
debug_20
debug_19
debug_18
debug_17
debug_16
debug_15
debug_14
debug_13
debug_12
debug_11
debug_10
debug_09
debug_08
debug_07
debug_06
debug_05
debug_04
debug_03
debug_02
debug_01
debug_00
TXD1
TXD2
TXD3
SCL
SDA
clk_sel1
clk_sel0
CLK_FUNC
CLK_STATUS
SCLK_CLK
MOSI_CLK
SEN_CLK
LED1
LED2
LED3
LED4
LED5
{SEN,MOSI,SCLK}_{TX_DB,TX_DAC,TX_ADC,DAC}
all moved from bank 3 (12 total lines)
R301
2.2K
R302
2.2K
SCL
SDA
DVDD_FPGA1
LED1
LED2
R311
R312
R314
R313
R682
XC3SD3400AFG676-BOTCLK
U1
CLK_FPGA_N
CLK_FPGA_P
exp_time_out_n
exp_time_out_p
exp_user_out_n
exp_user_out_p
USRP2-Plus FPGA Bank 2
$Date$
fpga-bank2.sch
11
12
Rev
$Author$

Bank 3, 3.3V
DAC
ADC
DB I/O
LSDAC, LSADC

FIXME −−− Check all MISO connections

Removed Vcco3 because of gnetlist bug

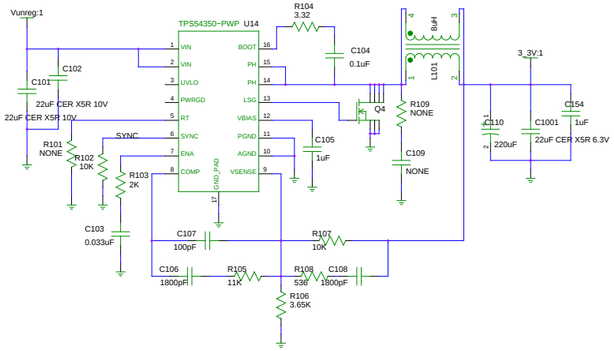


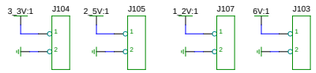


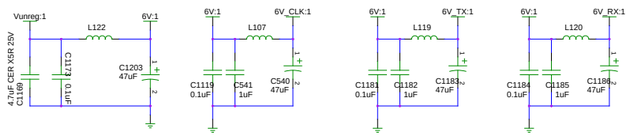
{SEN,MOSI,SCLK}_{TX_DB,TX_DAC,TX_ADC,DAC}
all moved to bank 2 (12 total lines)

USRP2−Plus FPGA Bank 3

TITLE	$Date$
FILE: fpga−bank3.sch	REVISION: Rev
PAGE 12 OF 12	DRAWN BY: $Author$

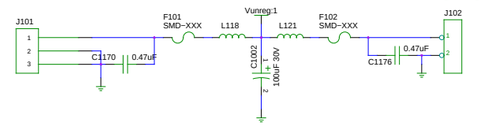






Front Panel Power

ALT Power



Power Supplies

6V Daughterboard Power (<1A), 5V for clock reg

3.3VCLK AD9510 (<500mA), Clock (88mA)

3.3VAN ADC (200mA), DAC (<500mA)

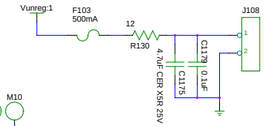
3.3VDIG All IO (<2A), FPGA AUX

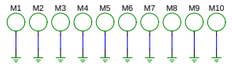
2.5V 1A −− Ethernet Core (600mA), SERDES (<150mA), RAM (<300mA)

1.2V FPGA Core (<2A)

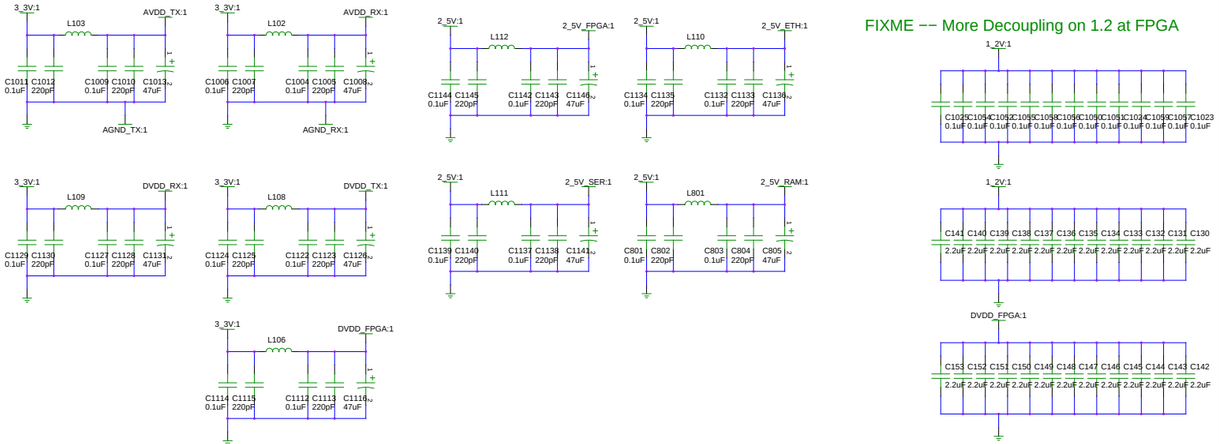
1.0V Ethernet Core

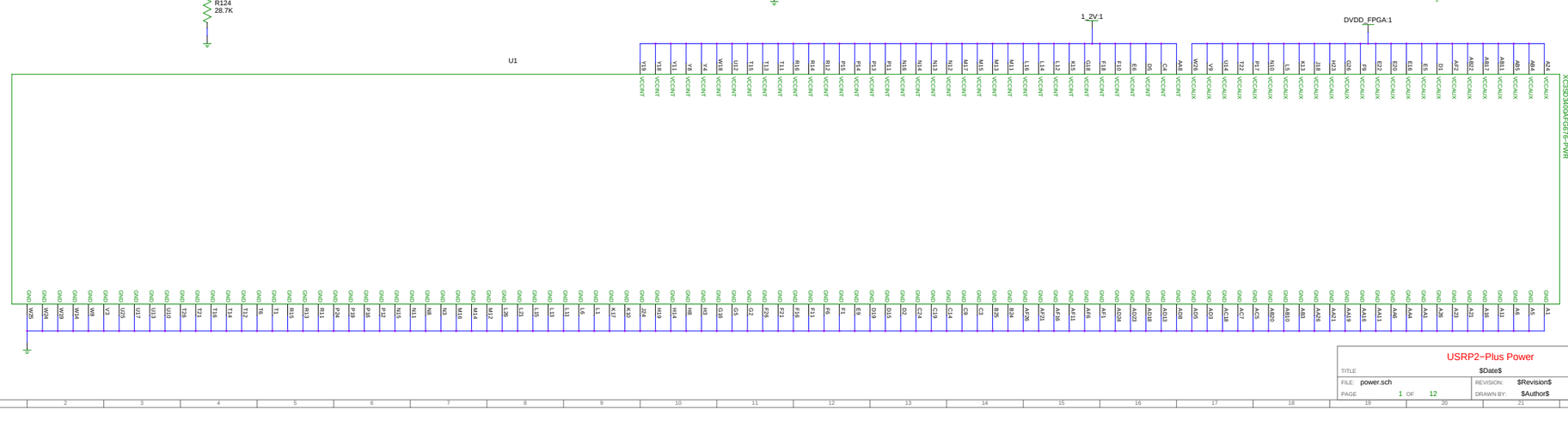
FAN Power





FIXME −− More Decoupling on 1.2 at FPGA





USRP2−Plus Power

TITLE: $Date$	
FILE: power.sch	REVISION: $Revision$
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