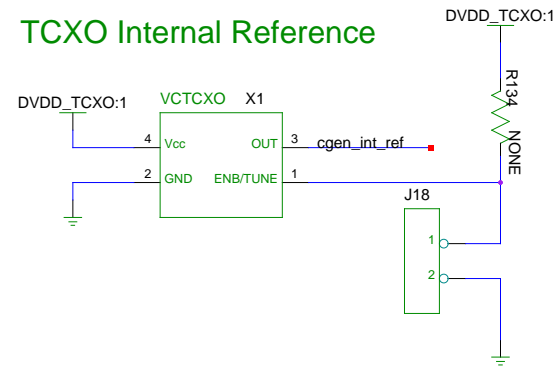
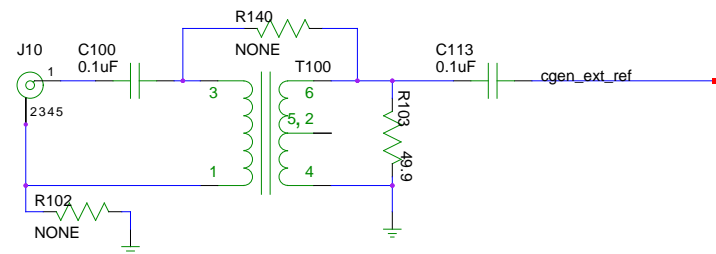


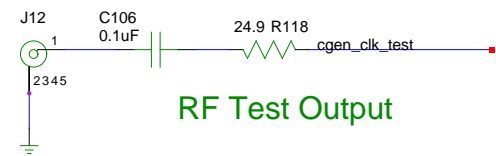
TCXO Internal Reference



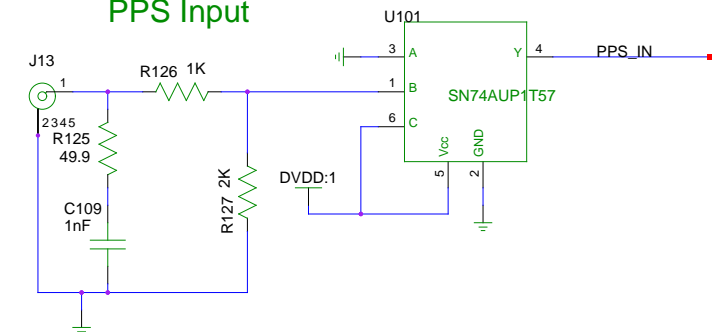
10MHz External Reference



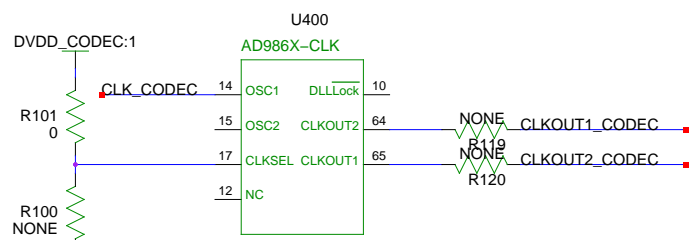
RF Test Output



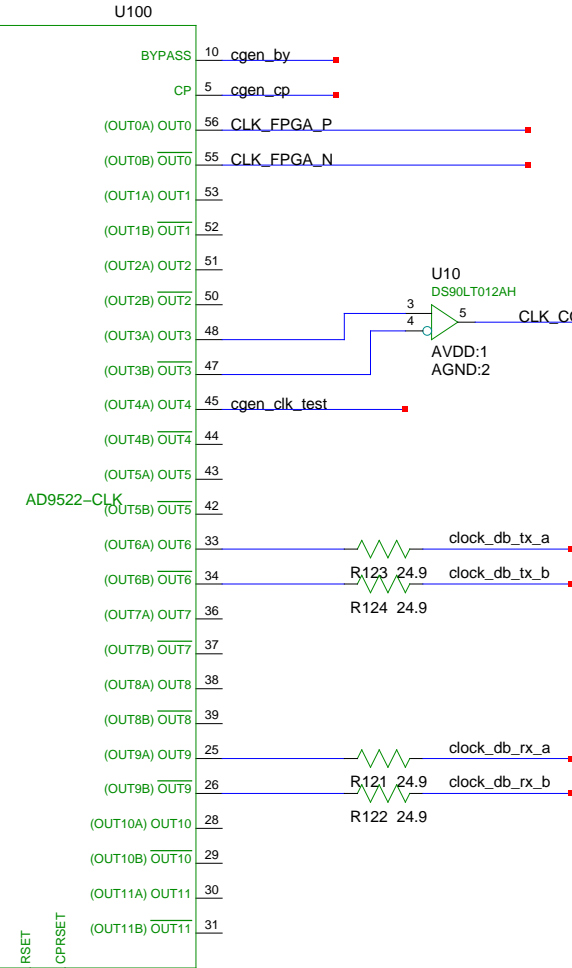
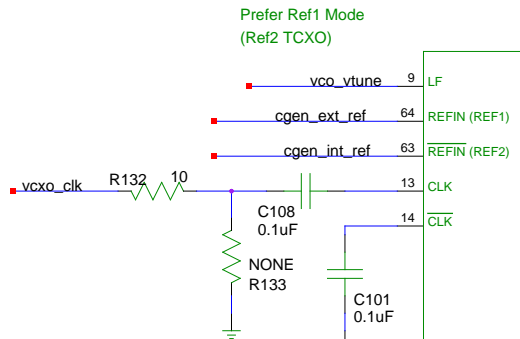
PPS Input



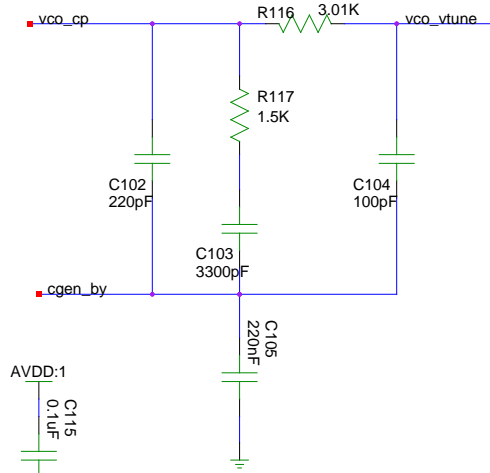
Make sure these resistors are close to U400



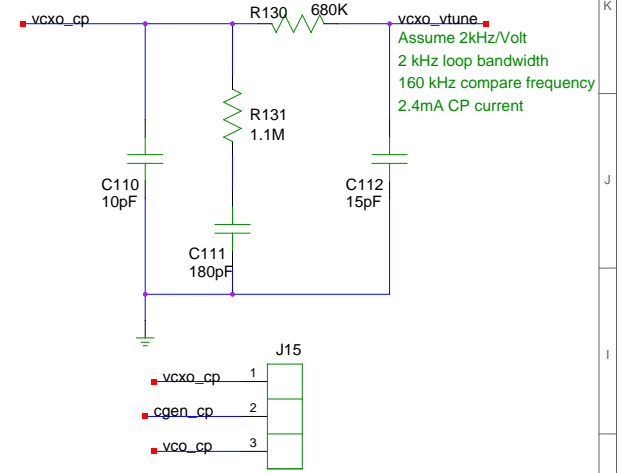
Prefer Ref1 Mode (Ref2 TCXO)



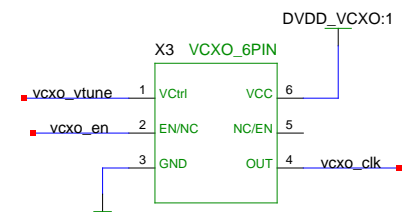
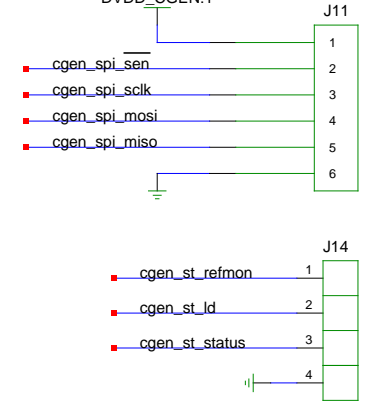
loop filter for internal VCO



loop filter for VCXO

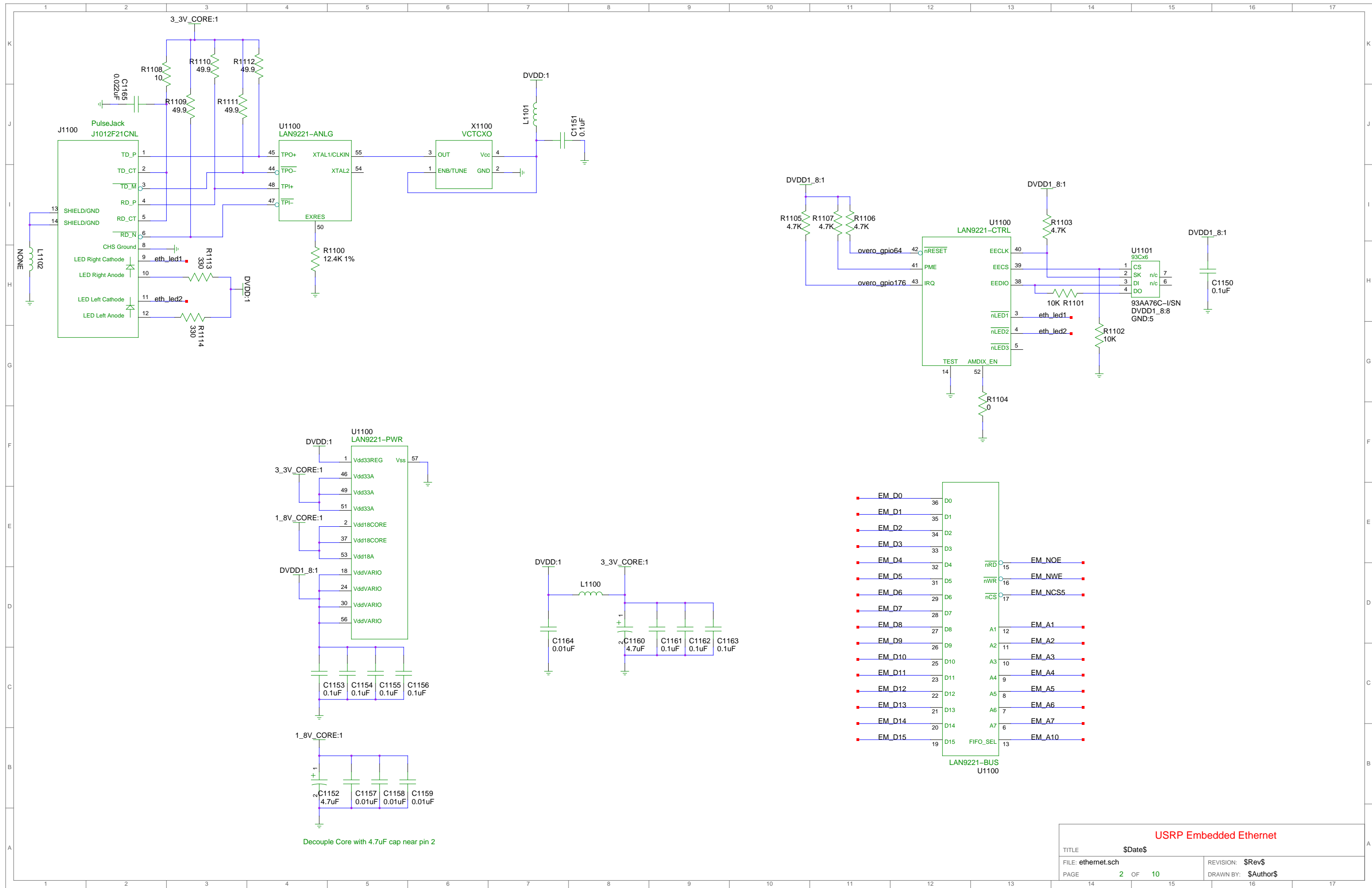


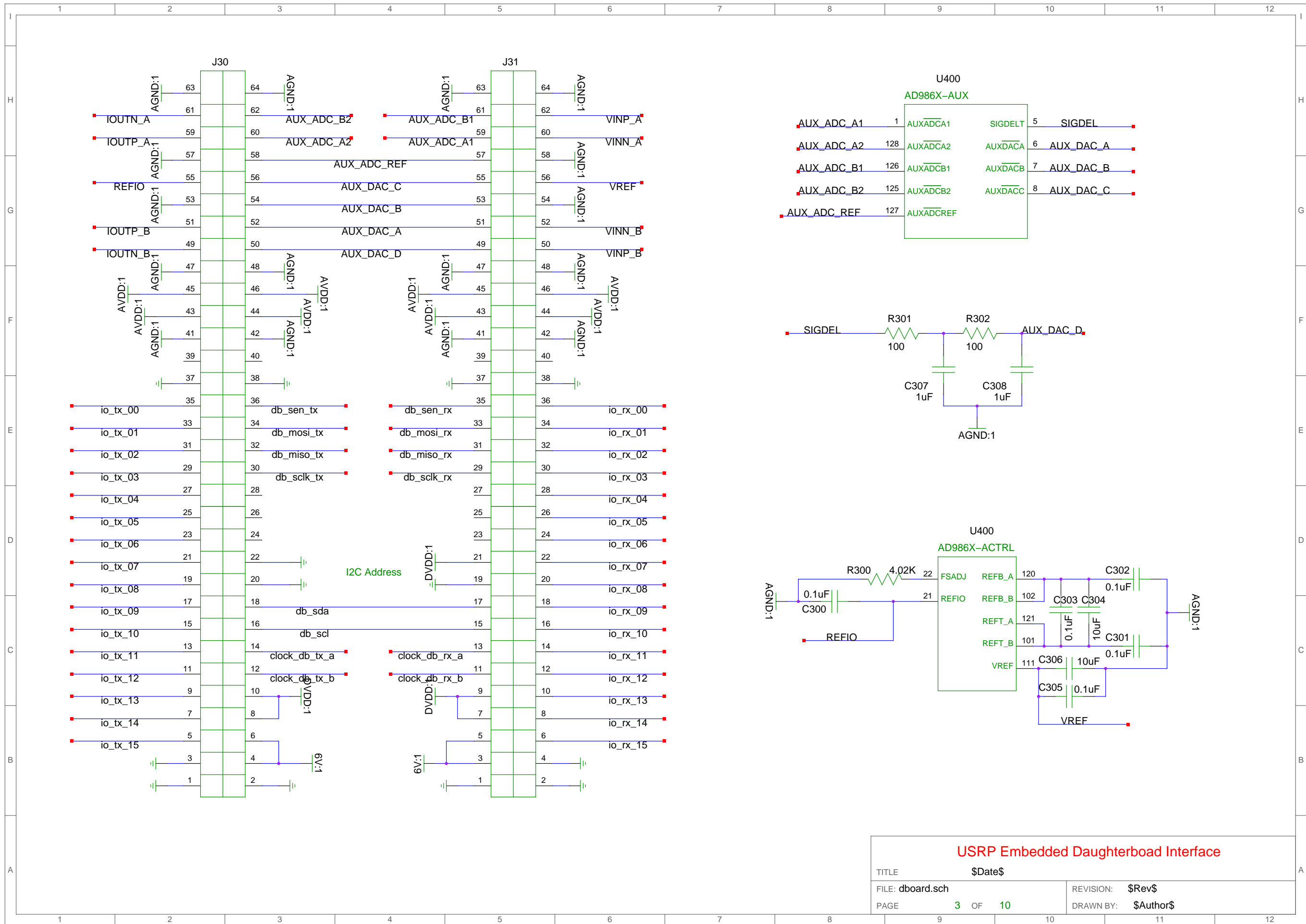
CGEN SPI Header



USRP Embedded Clock Generation

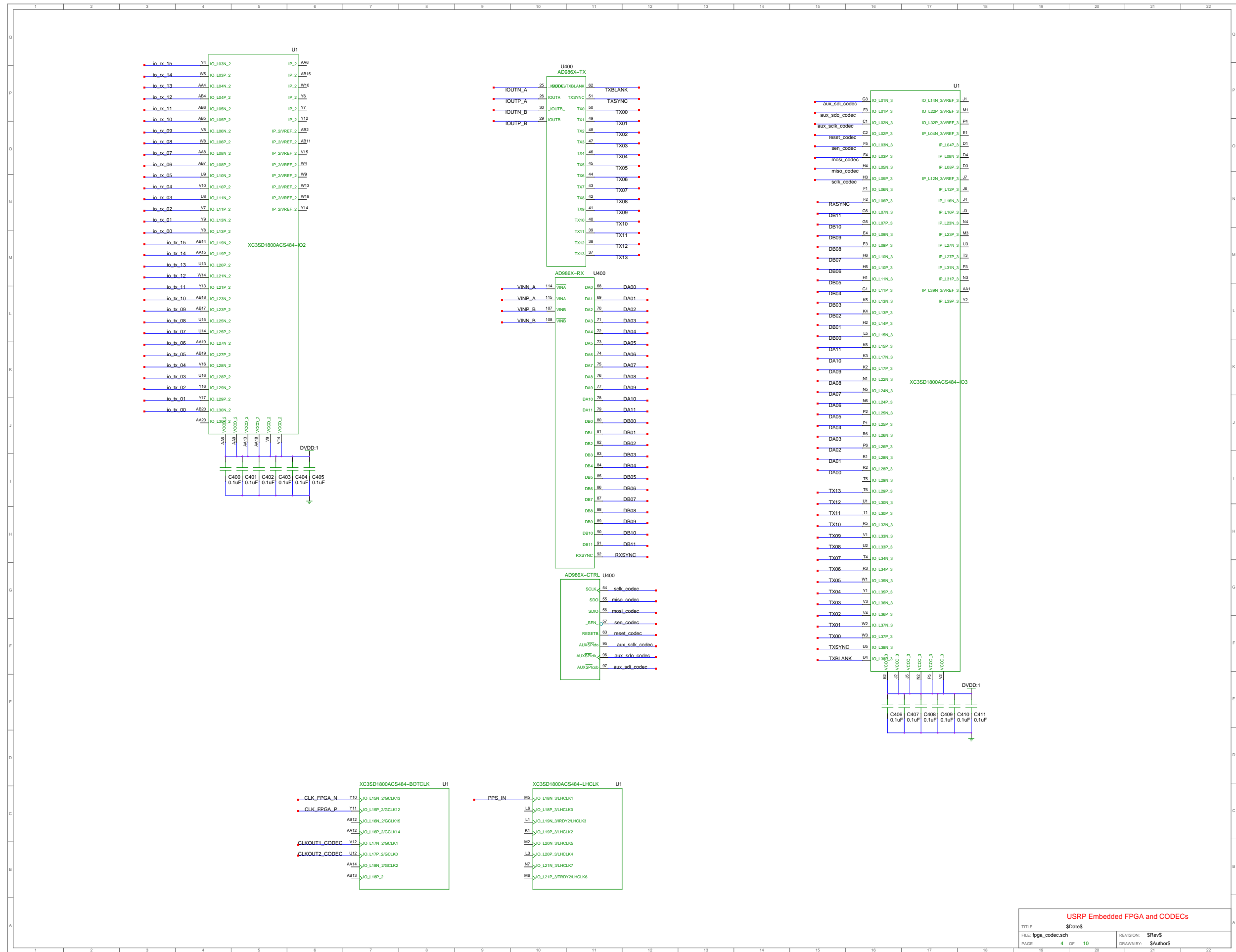
TITLE	\$Date\$	REVISION:	\$Rev\$
FILE:	clock.sch	DRAWN BY:	\$Author\$
PAGE	1 OF 10		



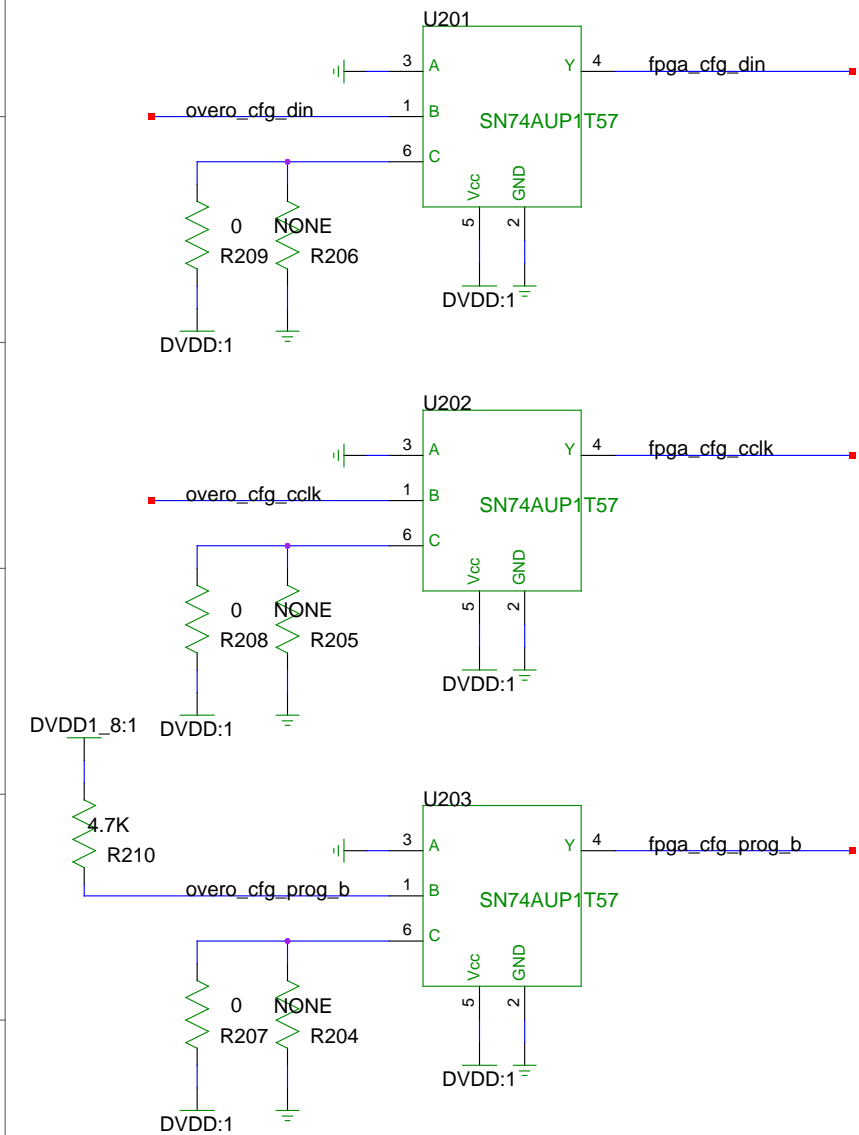


USRP Embedded Daughterboard Interface

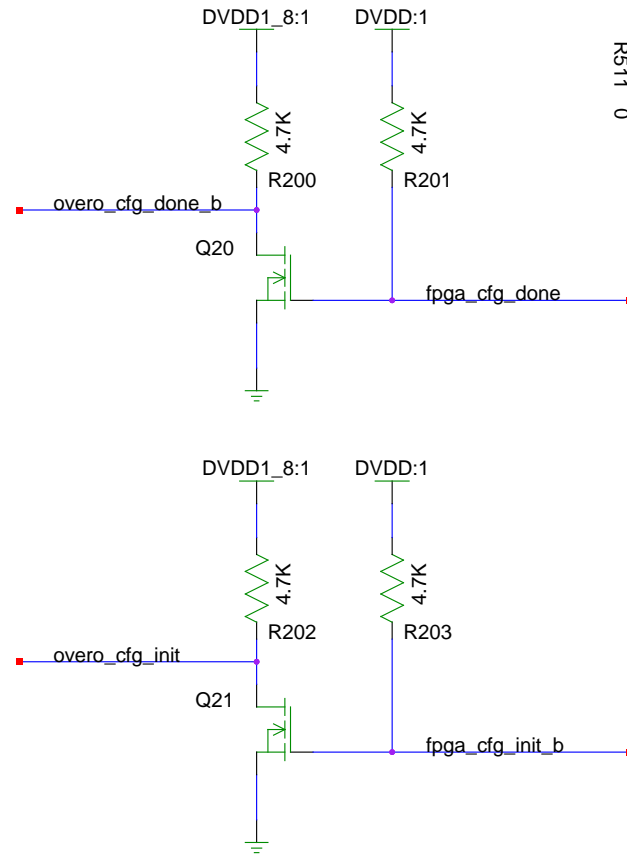
TITLE	\$Date\$	
FILE: dboard.sch	REVISION:	\$Rev\$
PAGE 3 OF 10	DRAWN BY:	\$Author\$



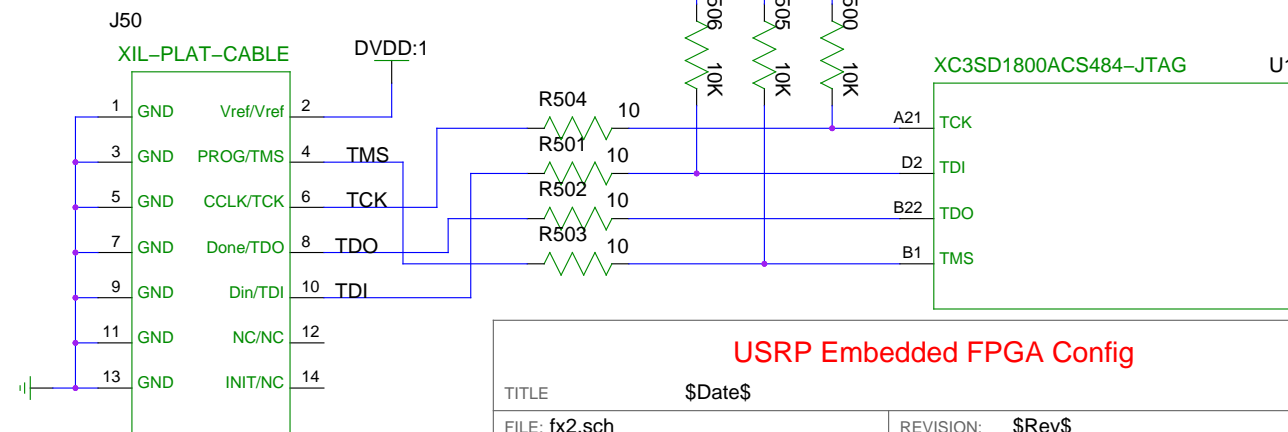
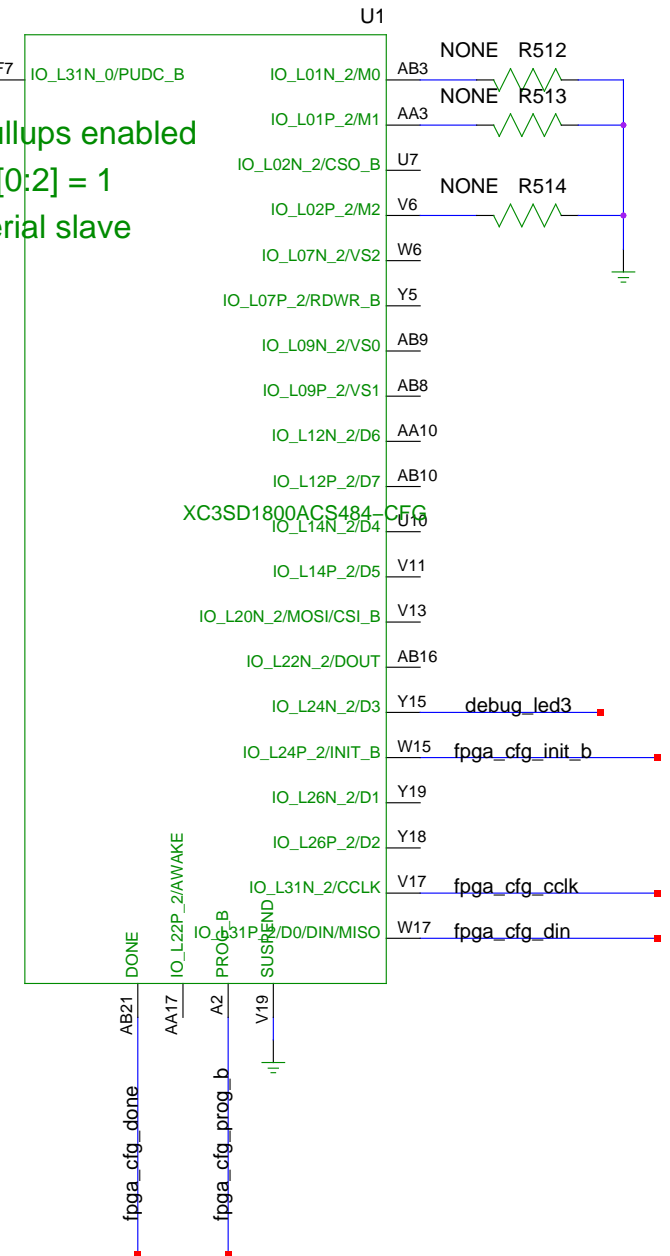
convert fpga config inputs



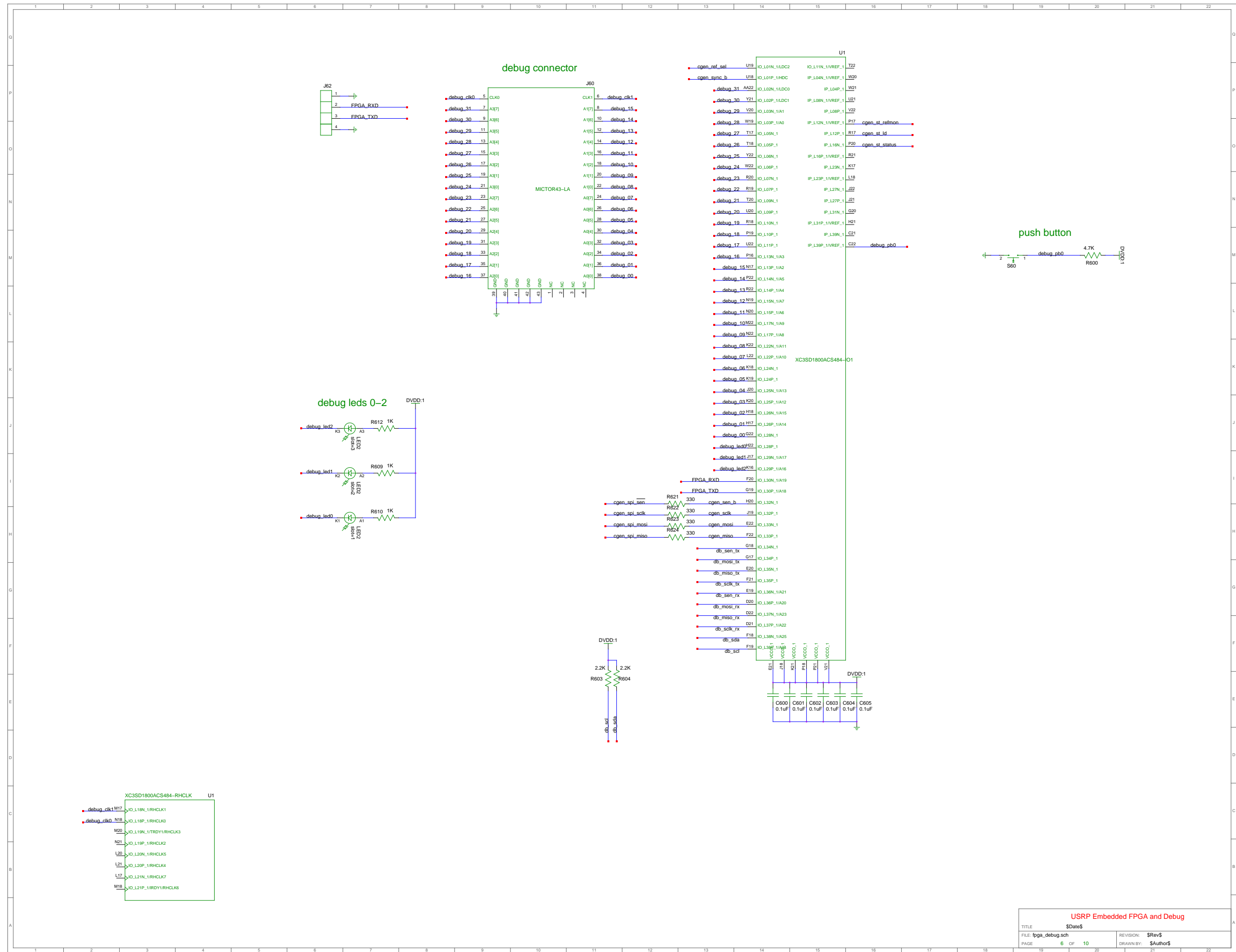
convert fpga config outputs

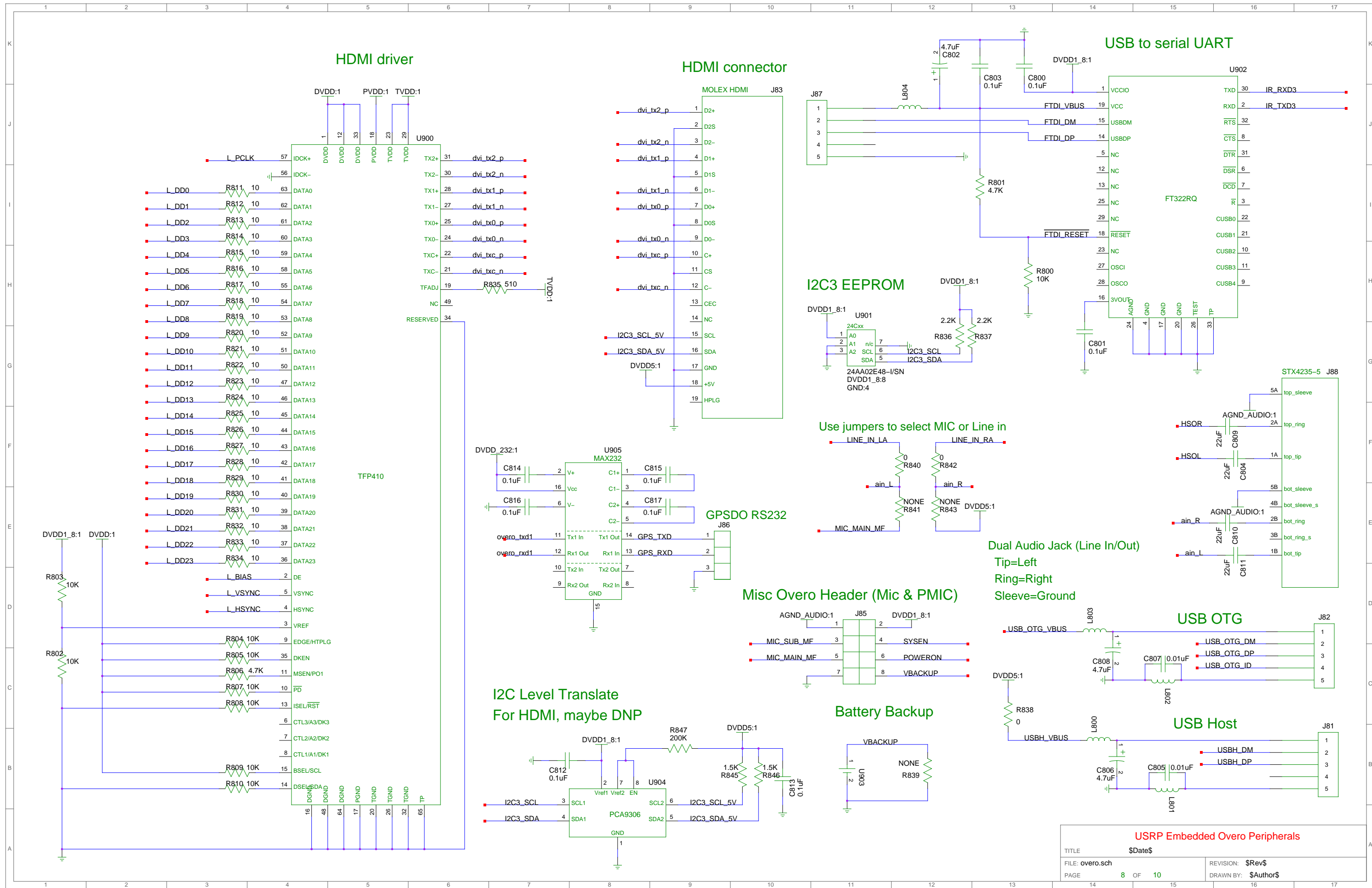


pullups enabled
m[0:2] = 1
serial slave

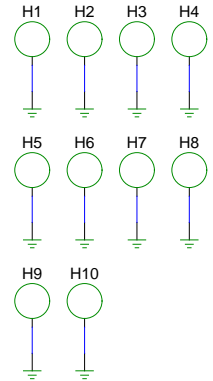
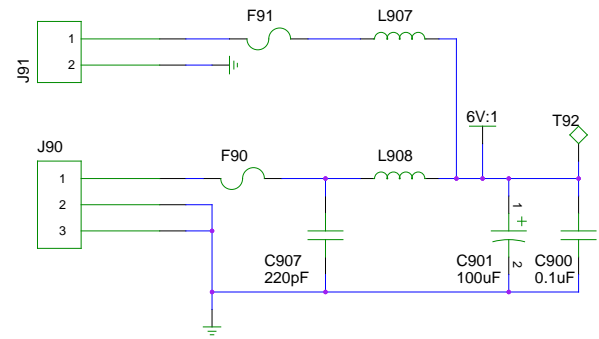


USRP Embedded FPGA Config

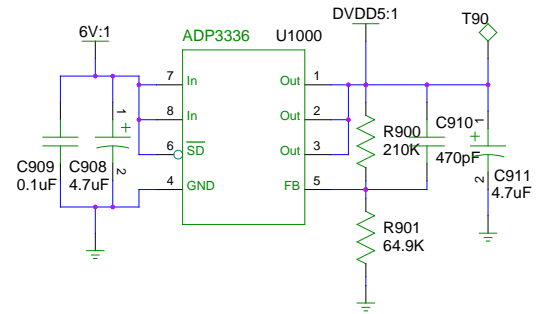




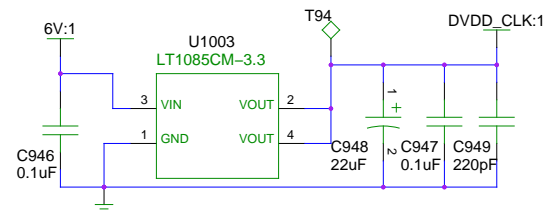
power supply 6v



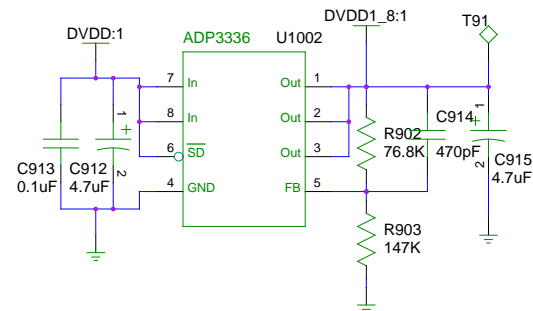
usb host and hdmi connector 5v



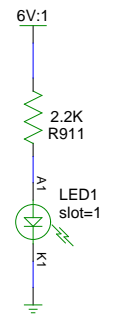
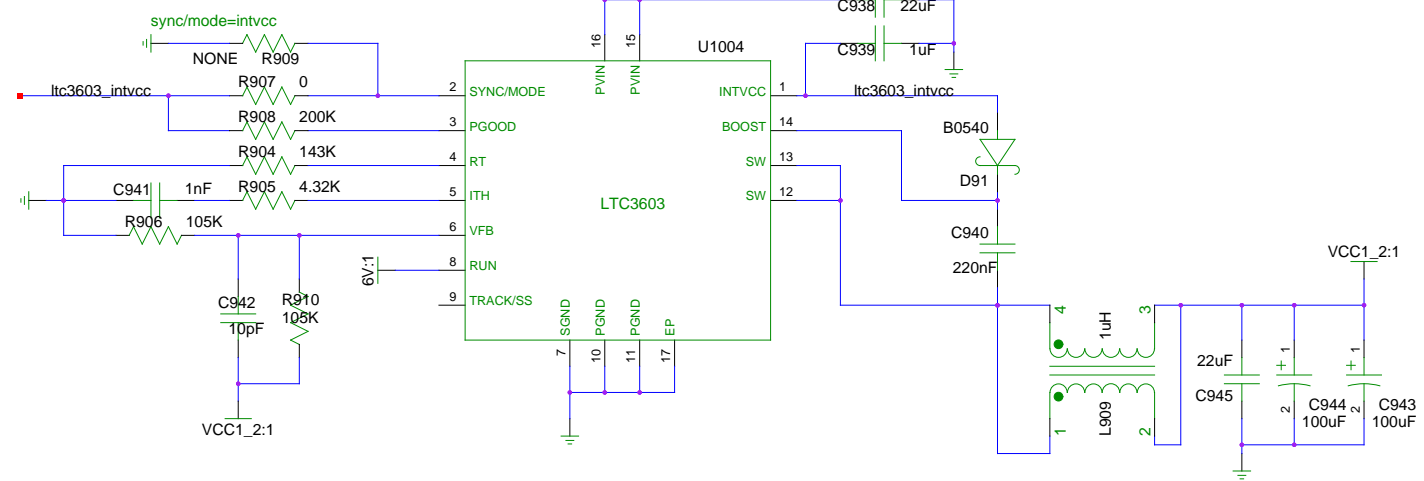
clock 3.3v



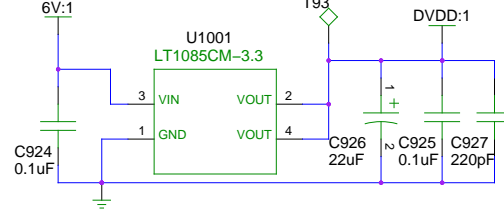
overo gpio 1.8v



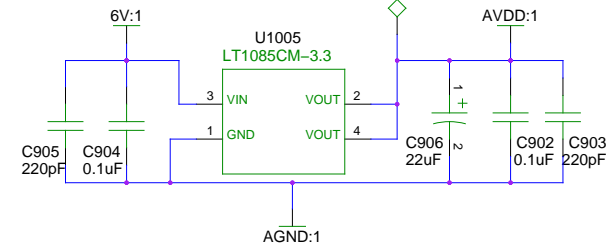
fpga internal 1.2v



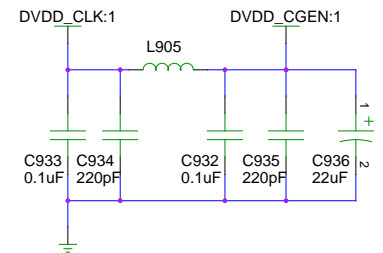
digital 3.3v



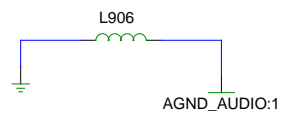
analog 3.3v



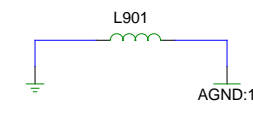
clock gen 3.3v



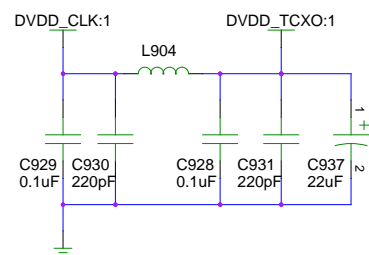
analog ground audio



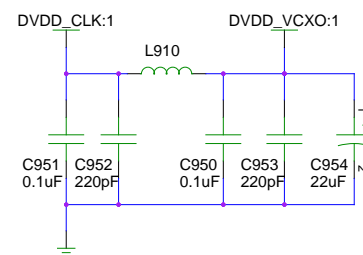
analog ground



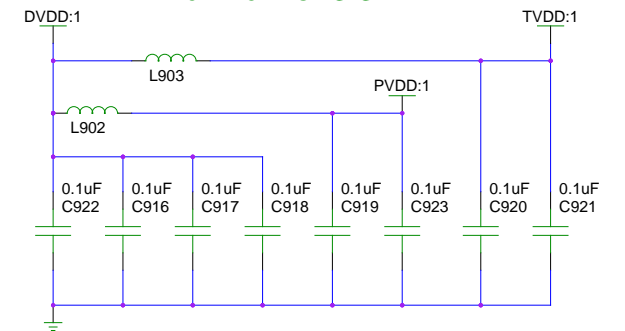
tcxo 3.3v



vcxo 3.3v



hdmi driver 3.3v



USRP Embedded Power Generation

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FILE:	power_gen.sch	DRAWN BY:	\$Author\$
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